

FIG. 1

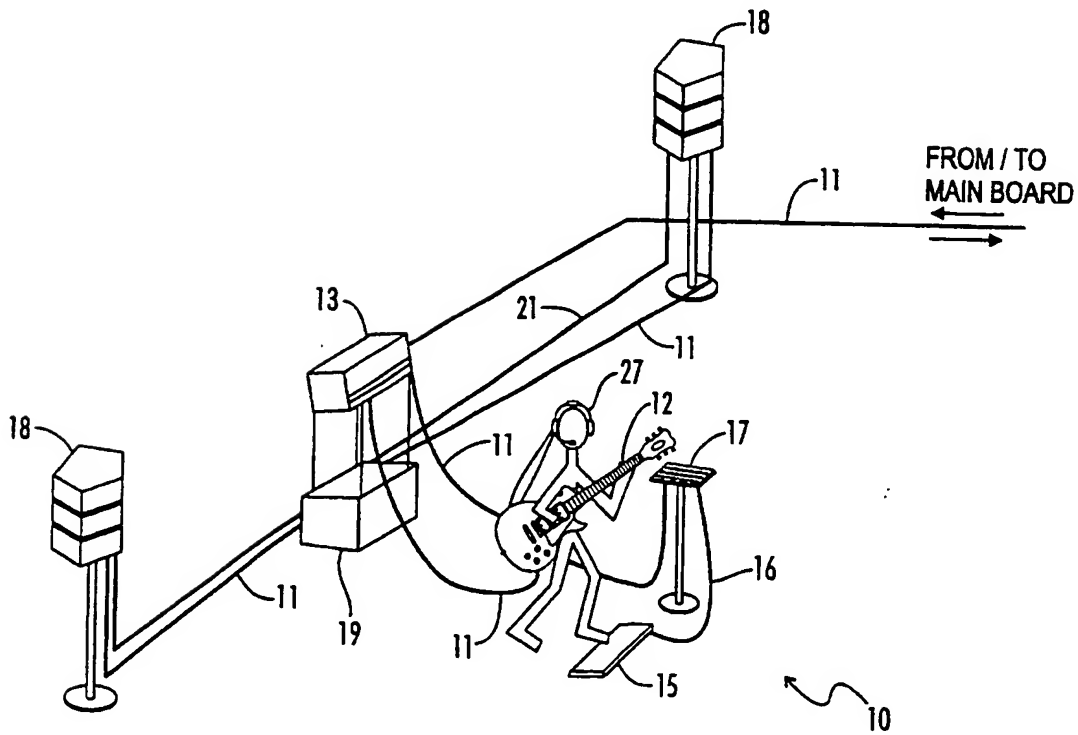


FIG. 2

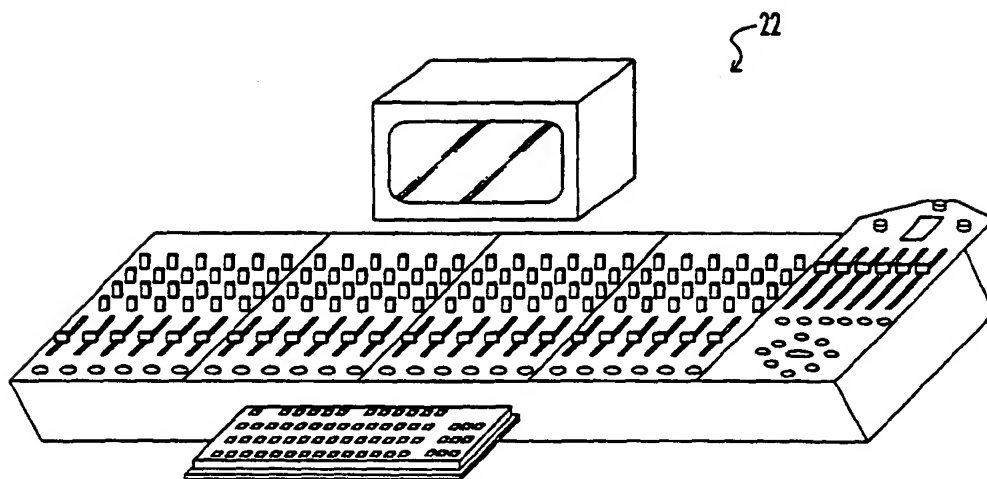


FIG. 3

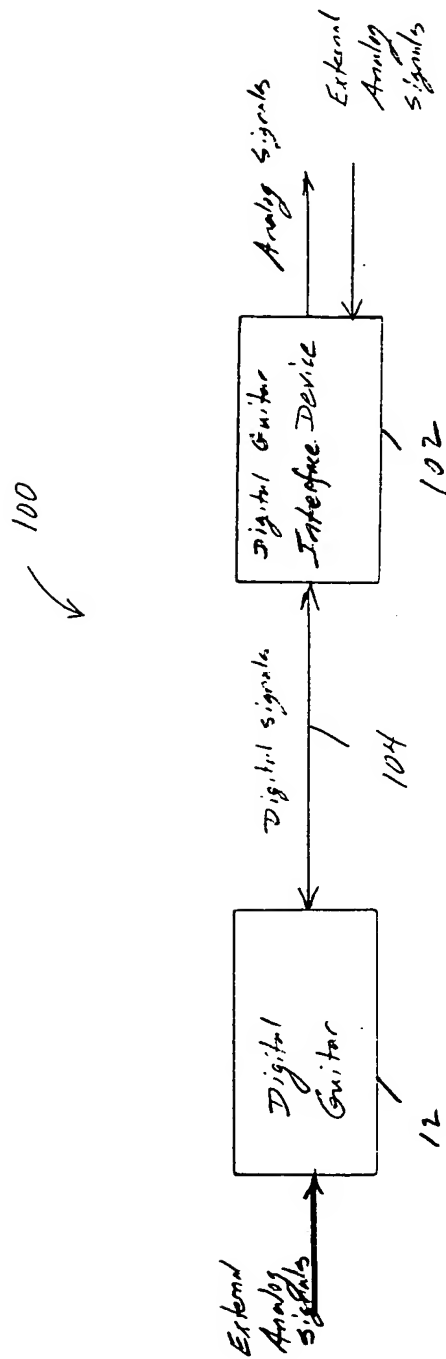


Fig. 4

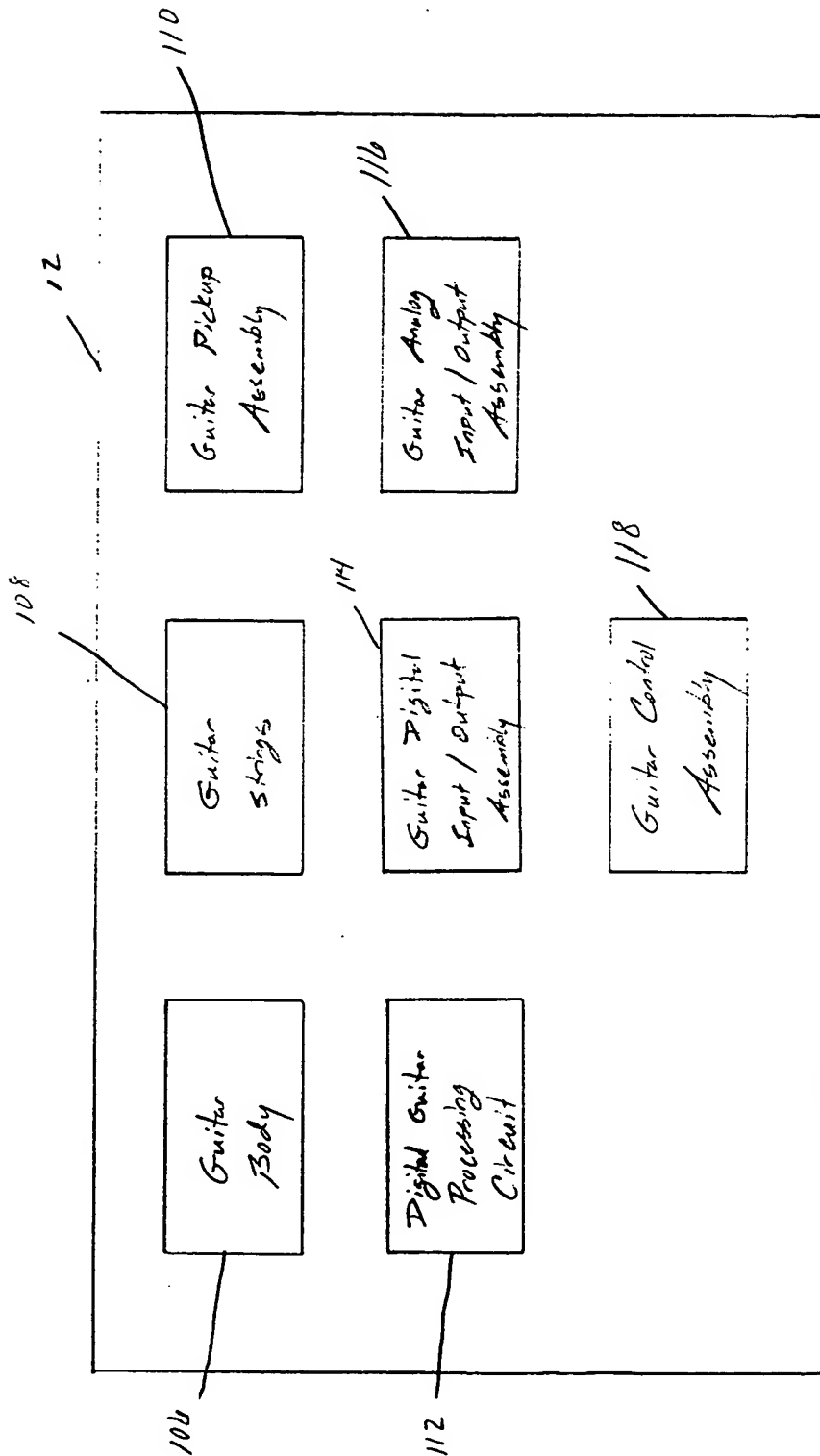


Fig. 5

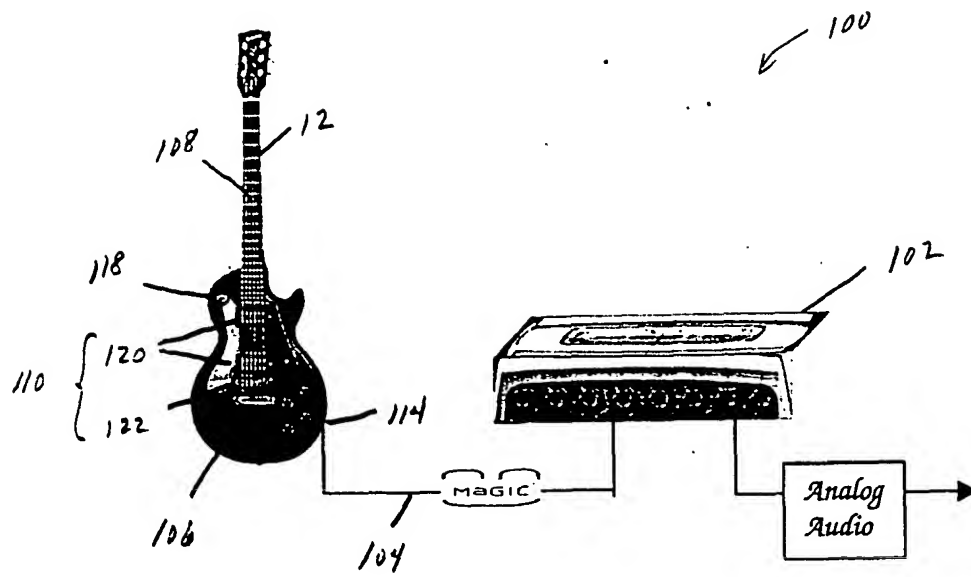


Figure 6

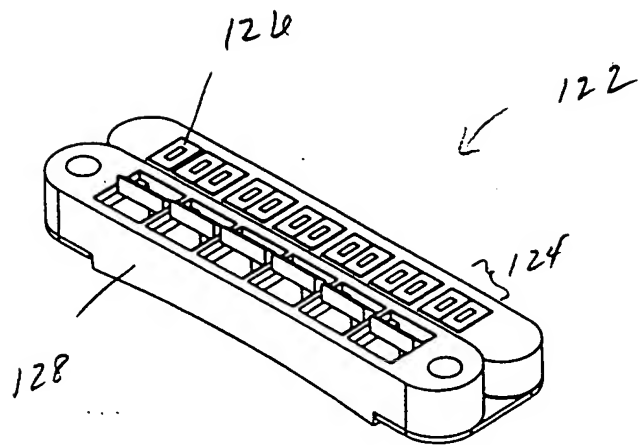
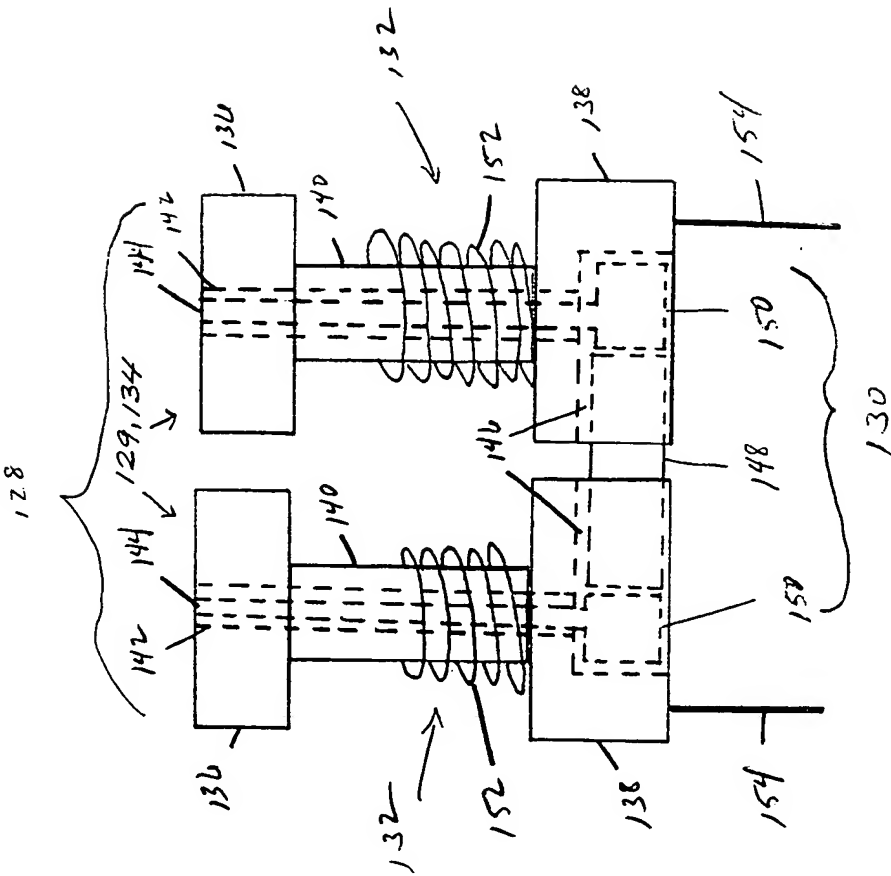


Fig. 7



Digital Guitar Processing Circuit 112

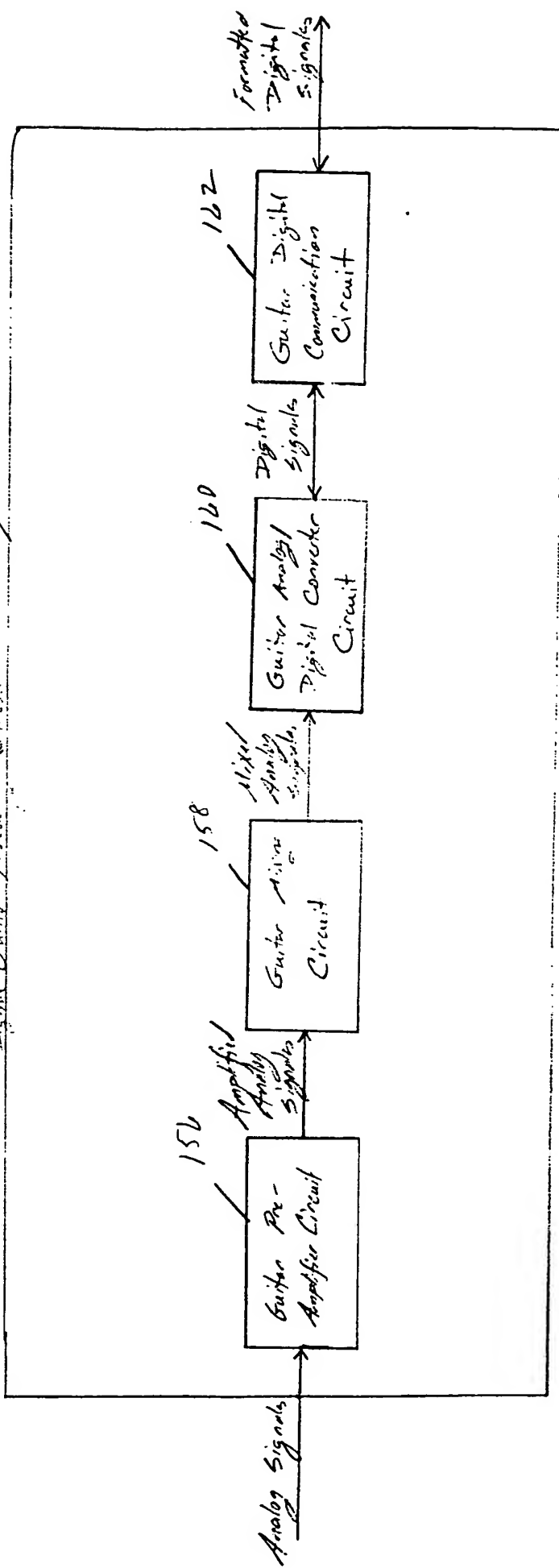


Fig. 9

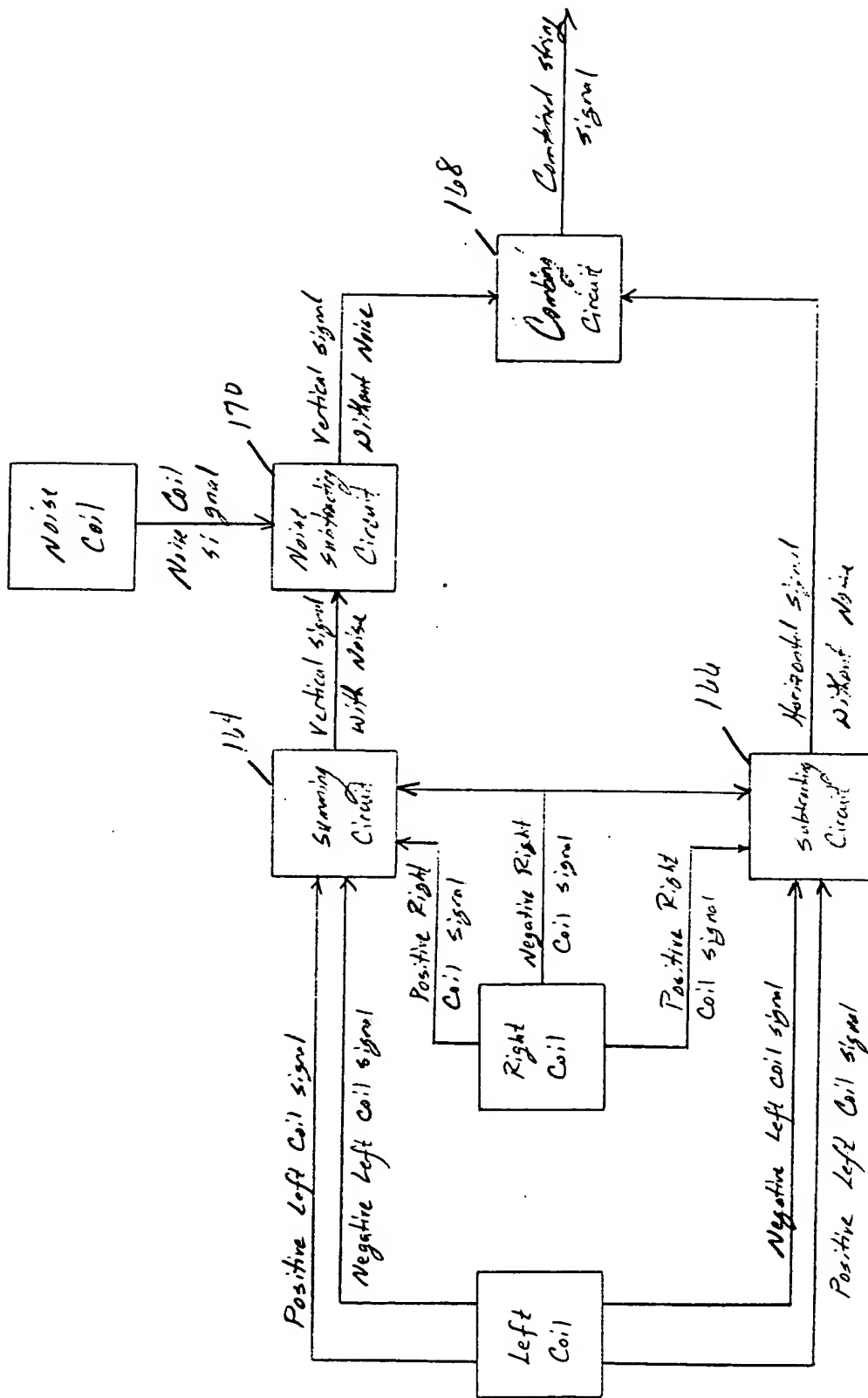


Fig. 10

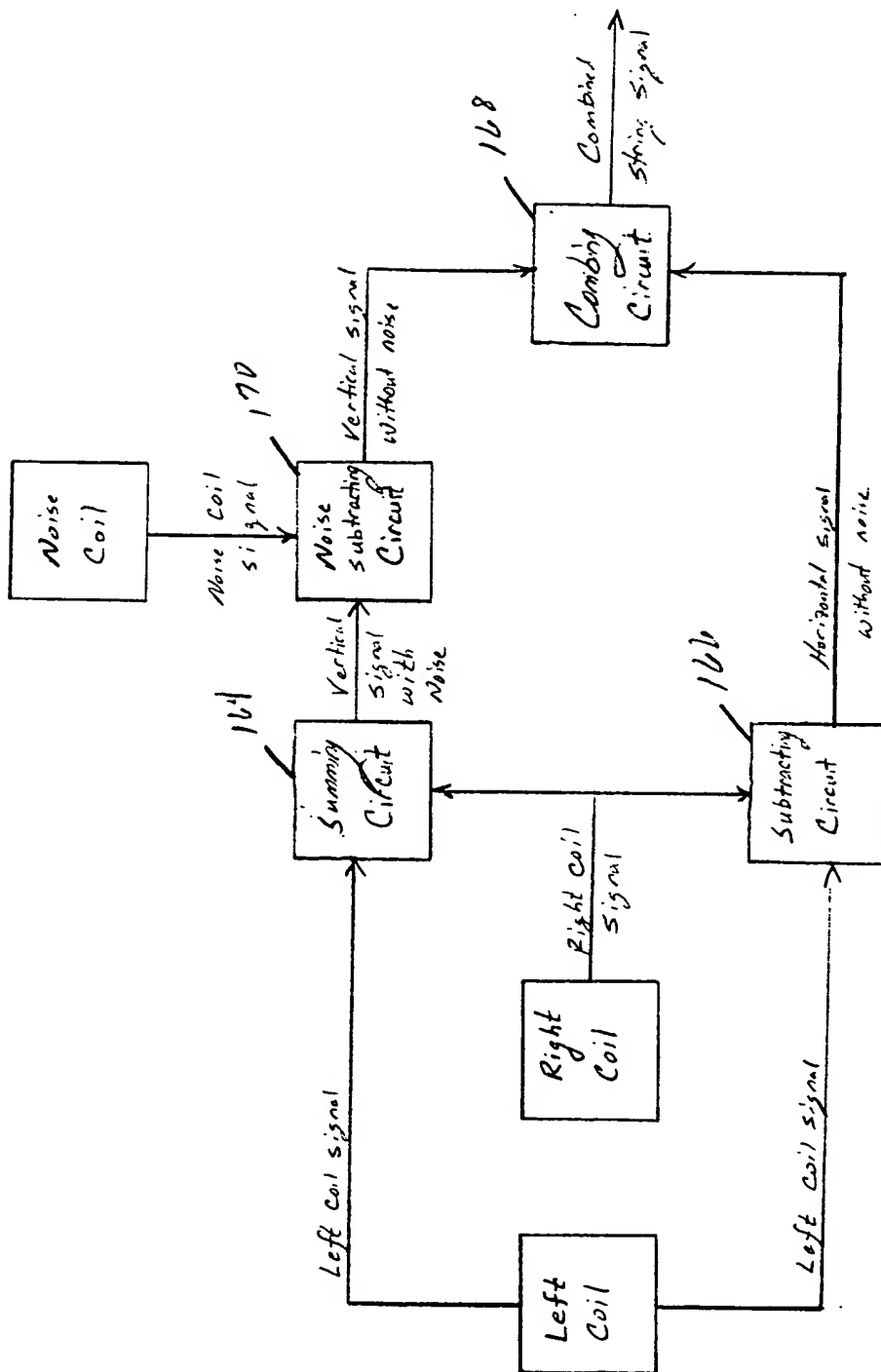


Fig. 11

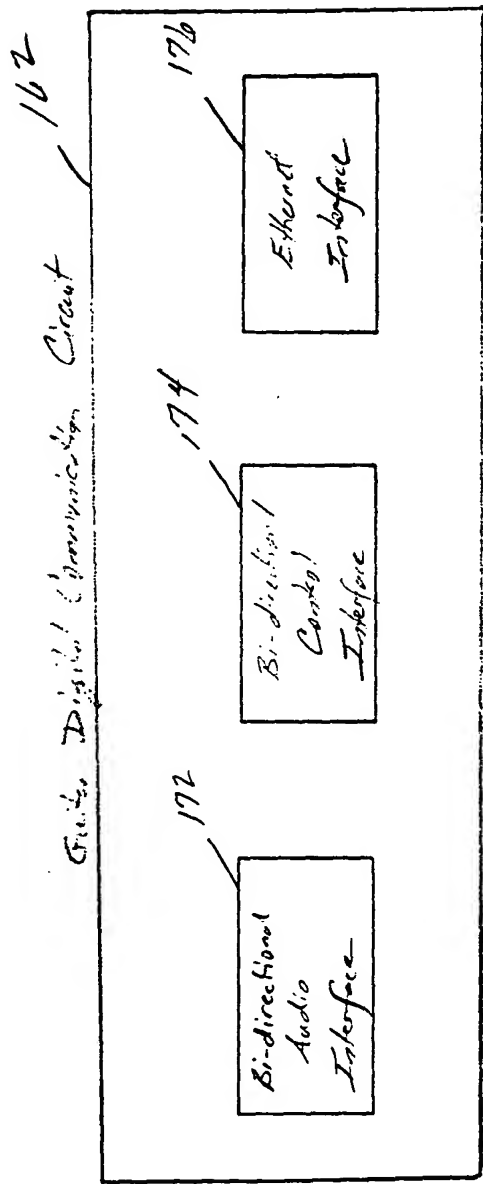


Fig 12

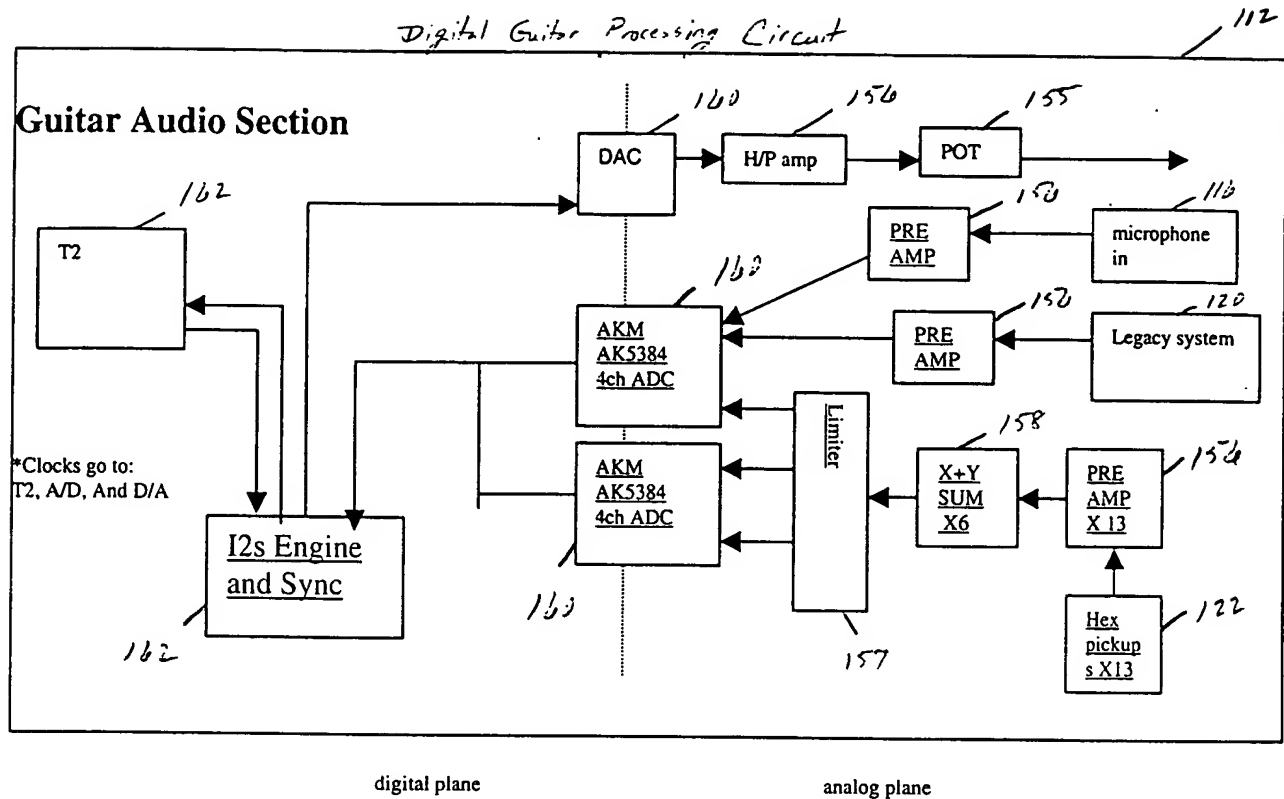


Figure 13

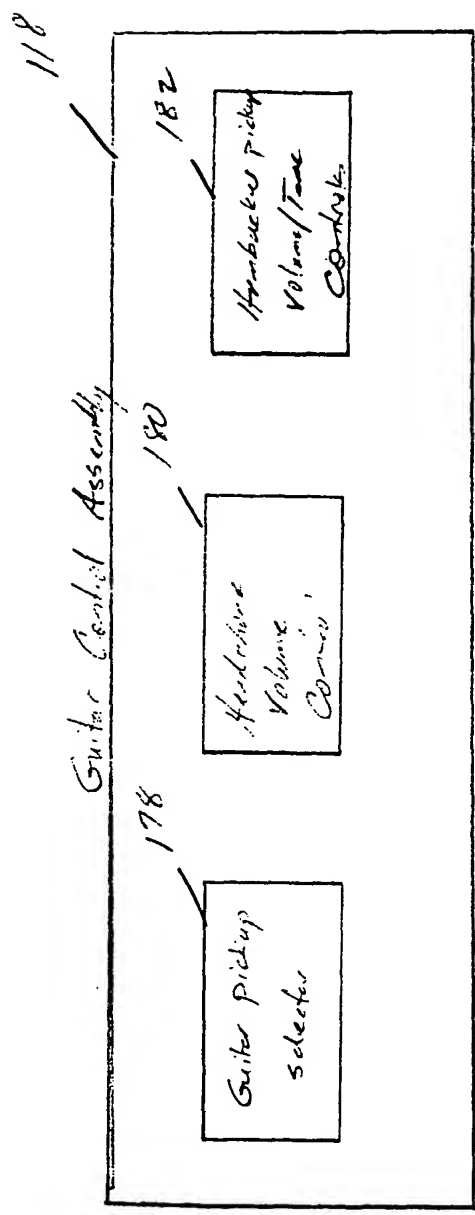


Fig. 17

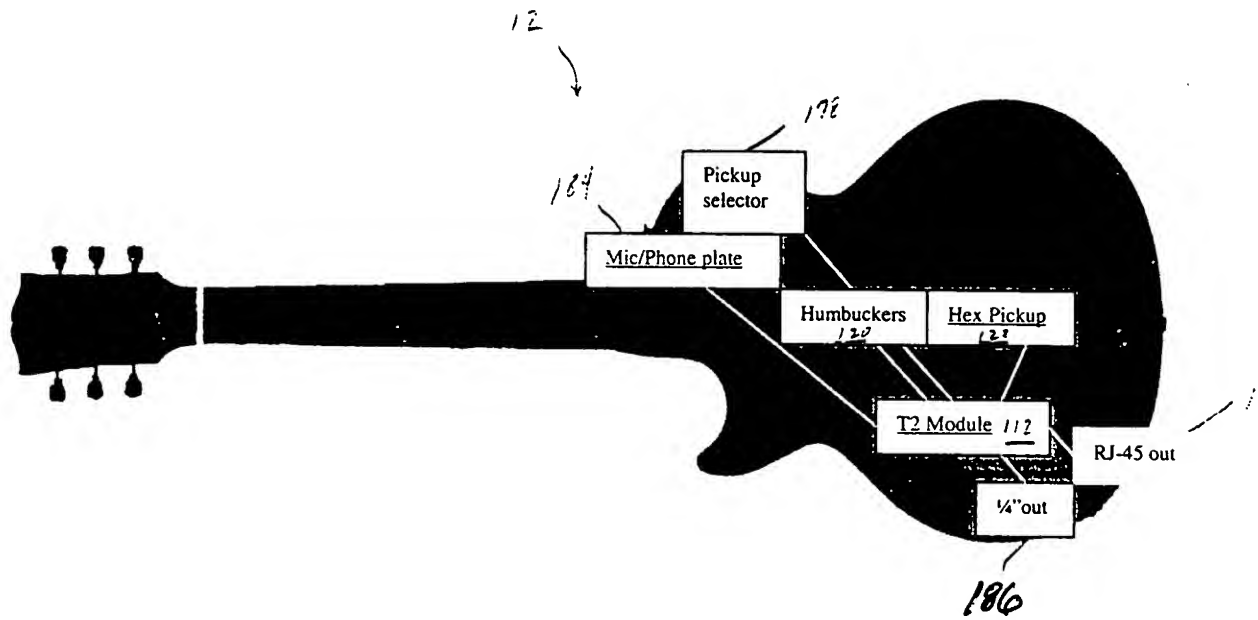


Figure 15

Preamp Section

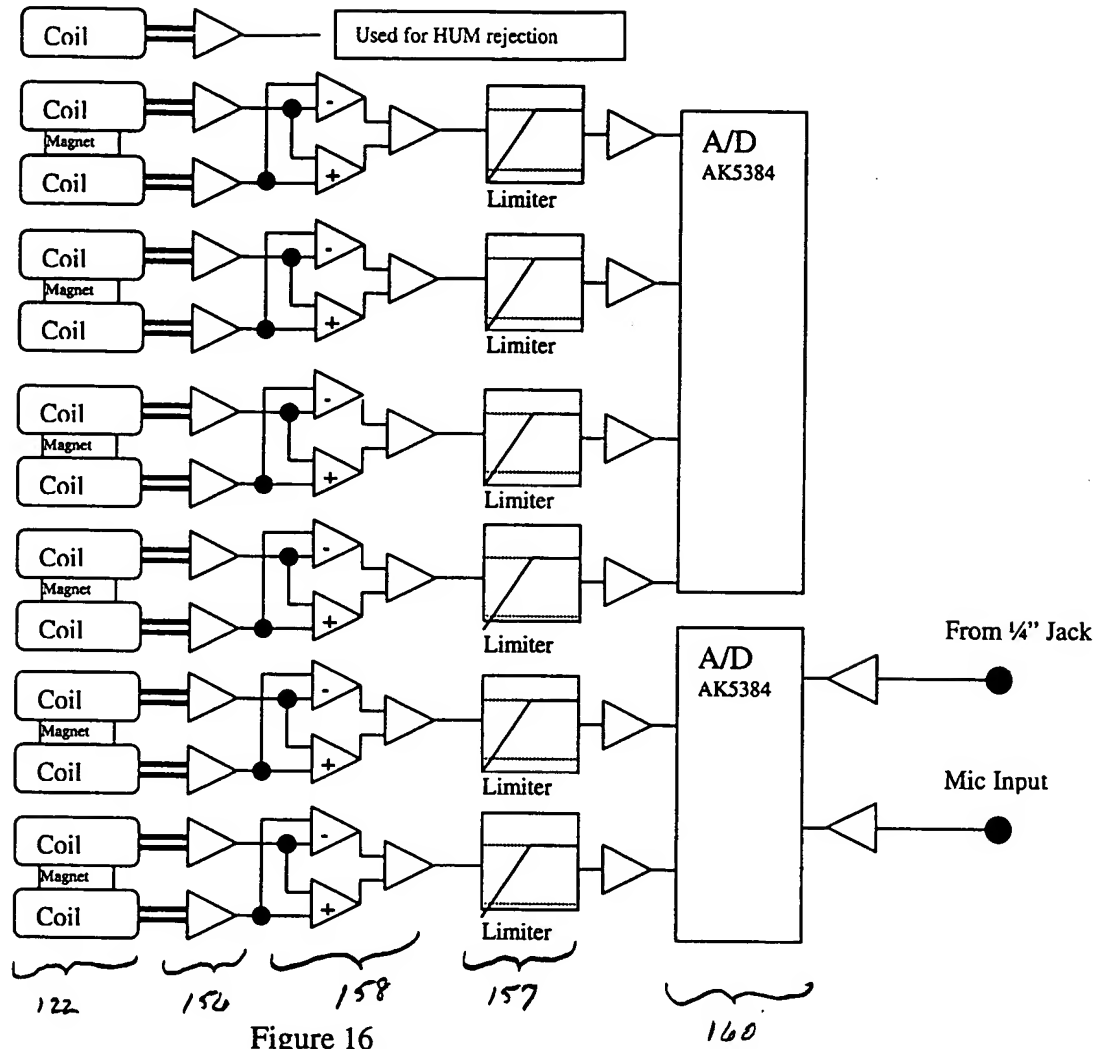


Figure 16

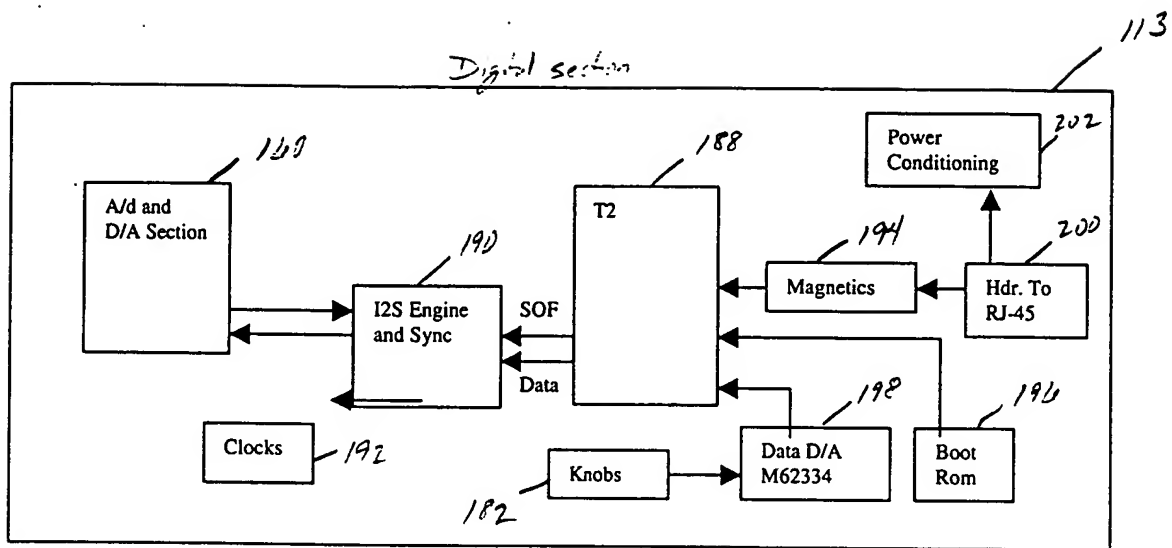


Figure 17

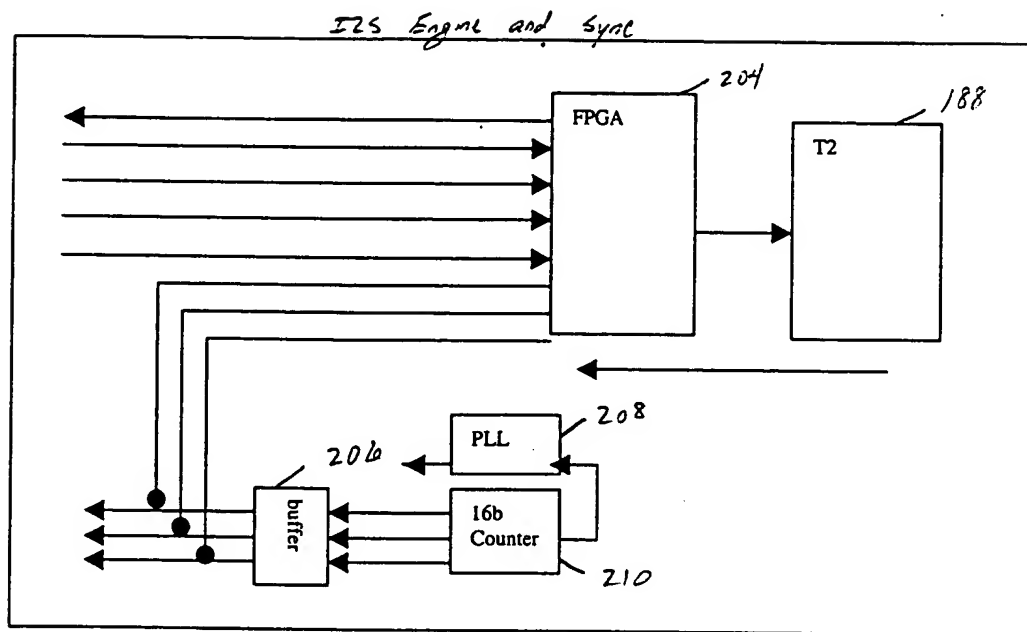


Figure 18

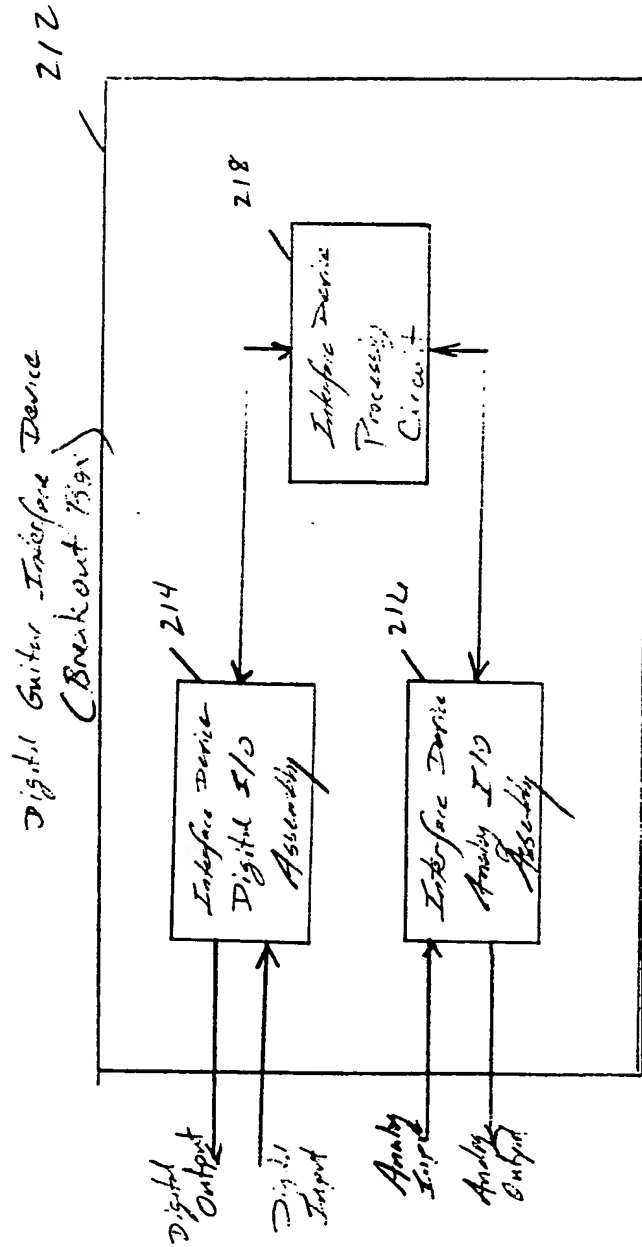


Fig. 19

Interface Device Processing Circuit

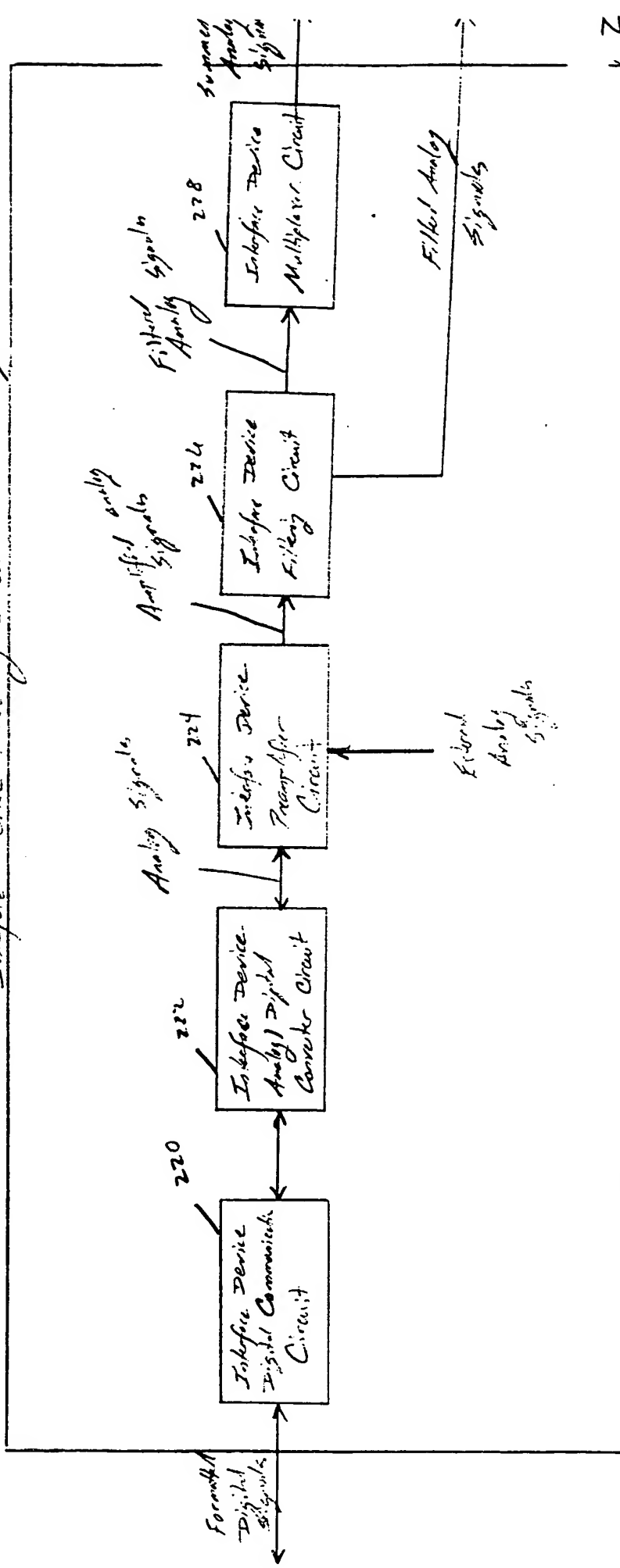
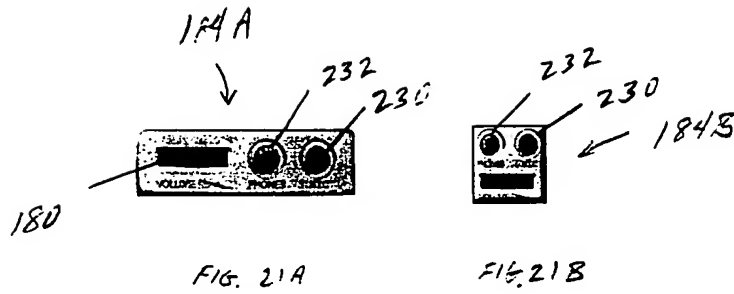


Fig. 20



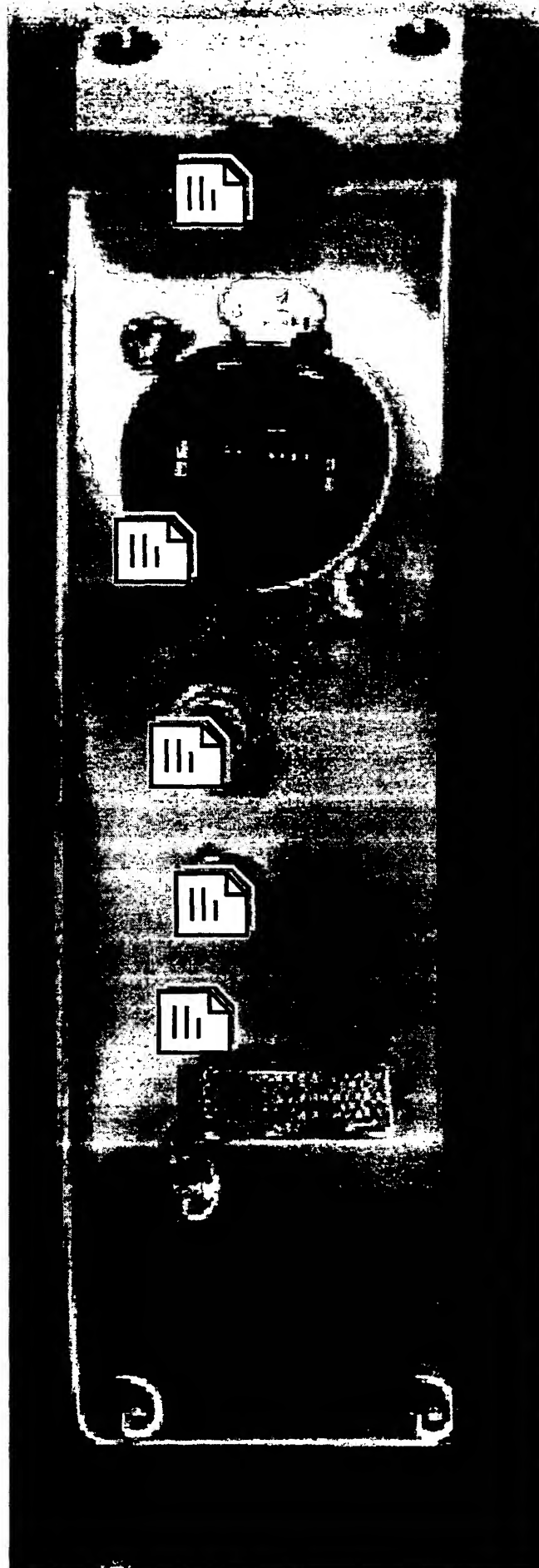


FIG. 21C

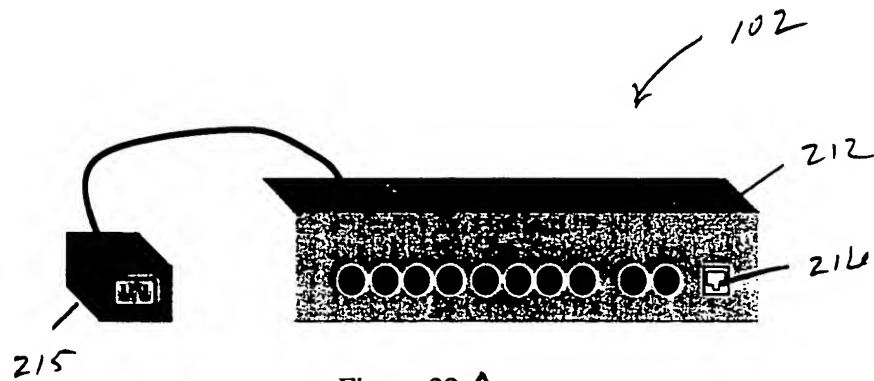


Figure 22 A

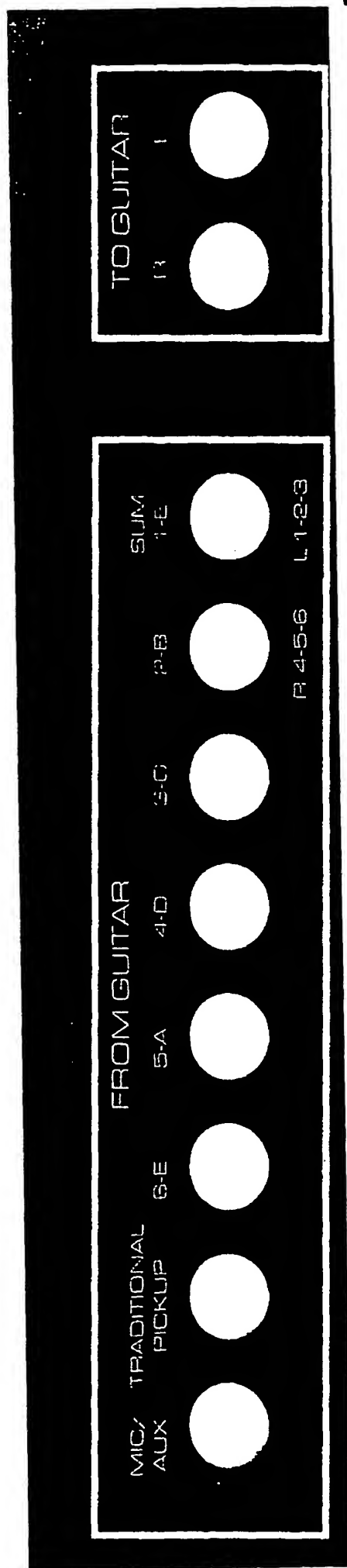


FIG. 22 B

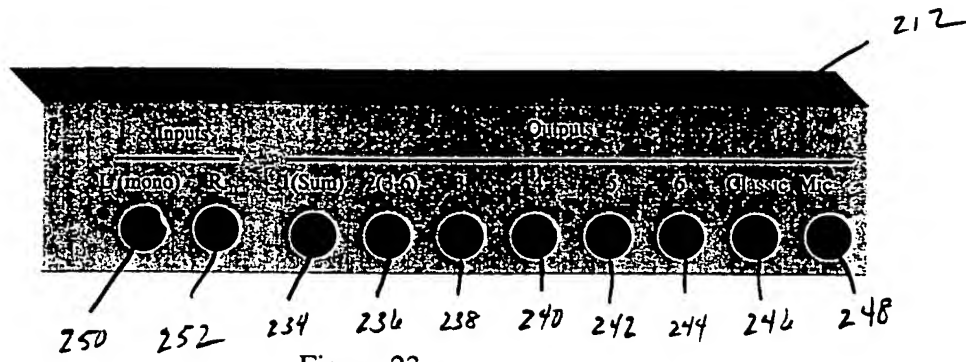


Figure 23

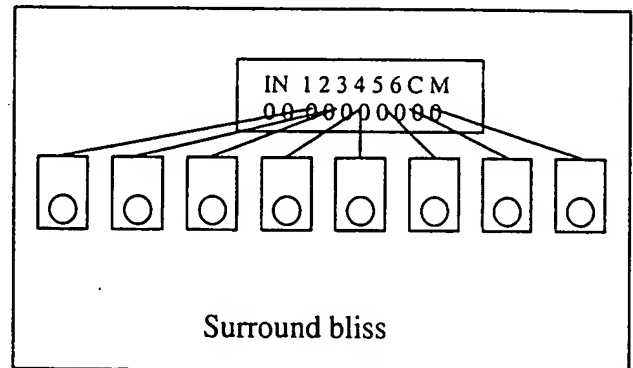
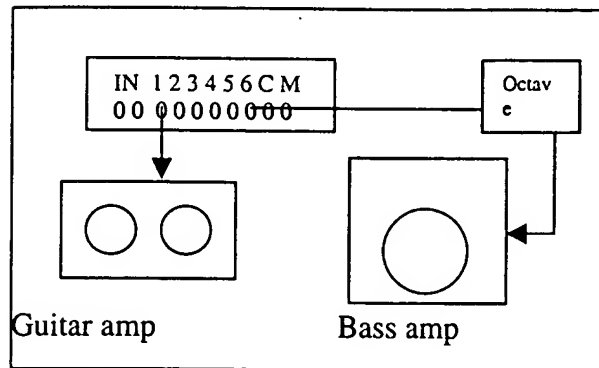
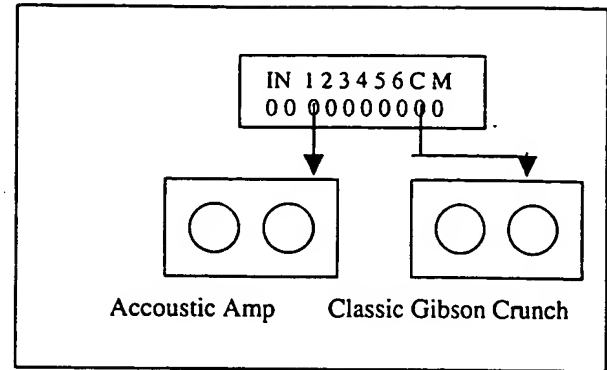
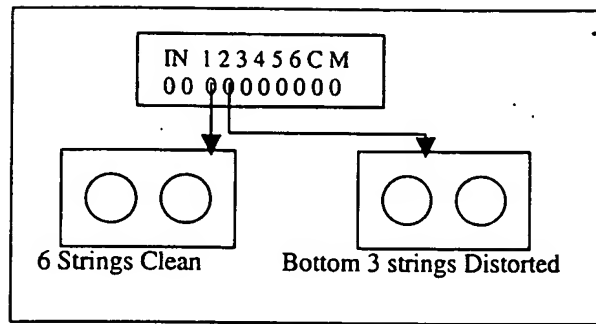


Figure 24

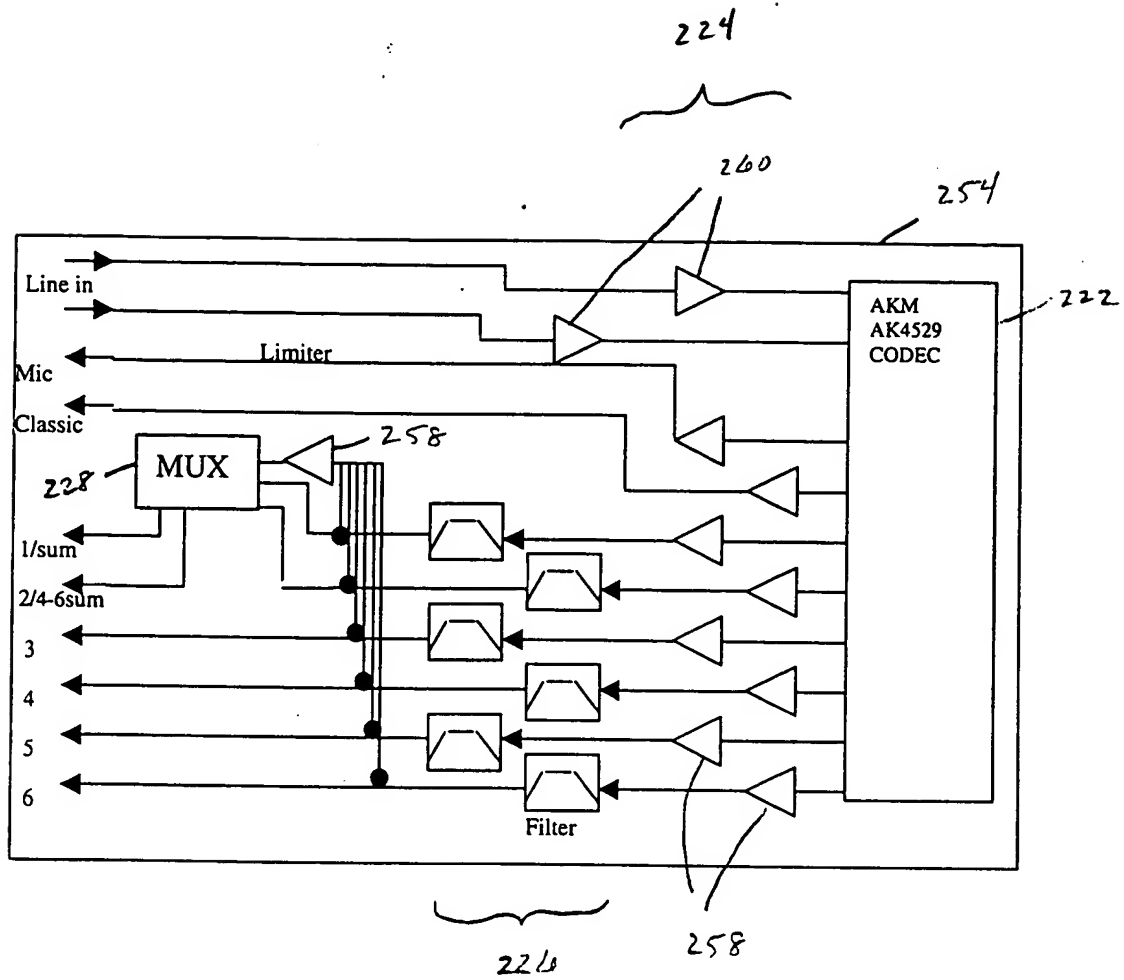


Figure 25

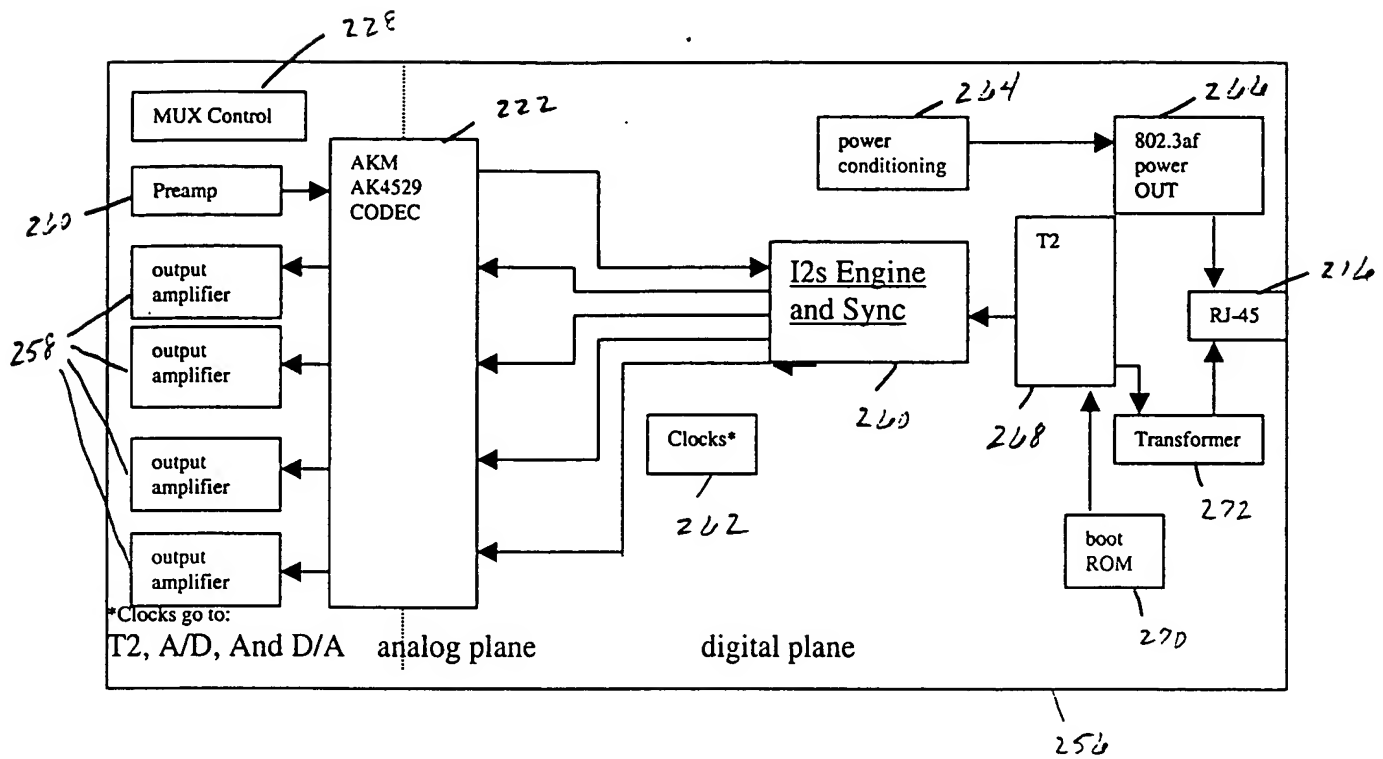


Figure 26

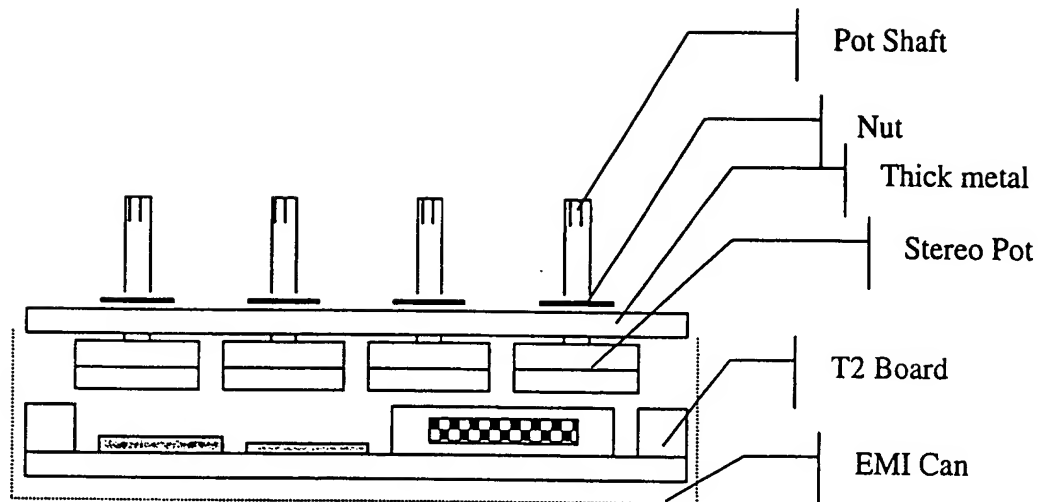
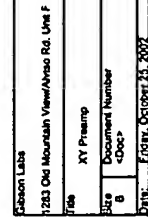


Figure 27

Figure 28

Clock Buffer

Phase Locked
Loop



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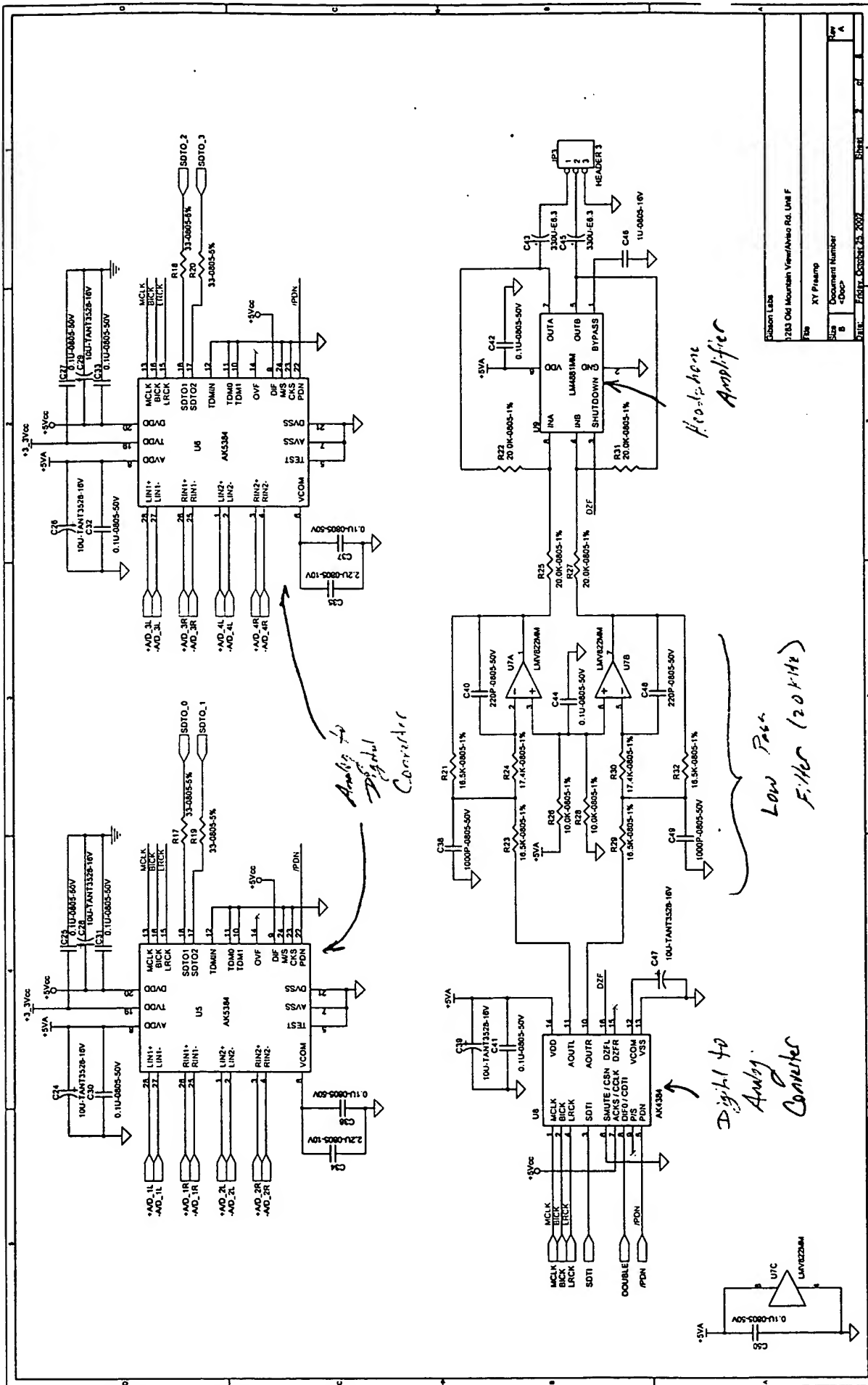
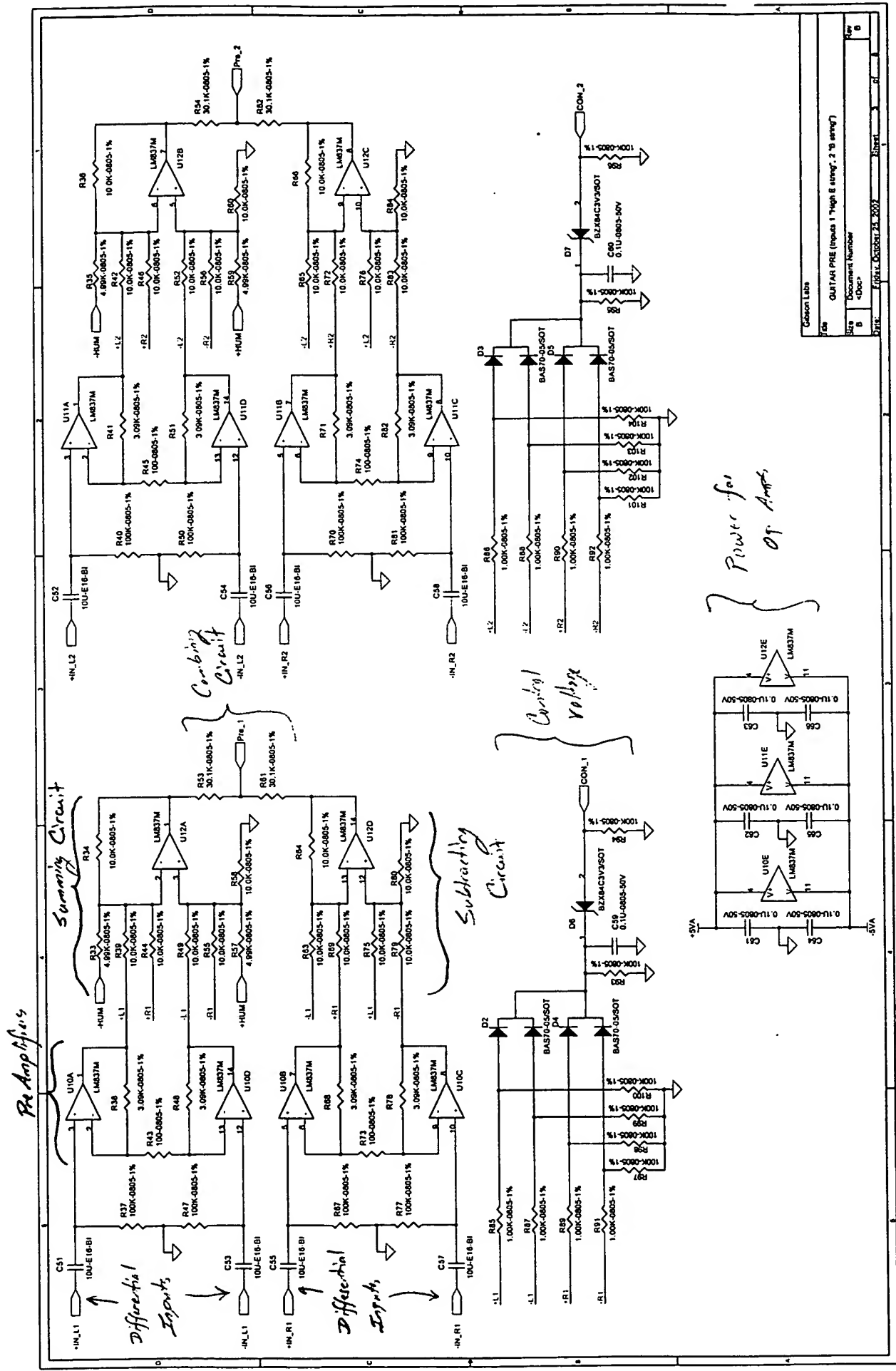
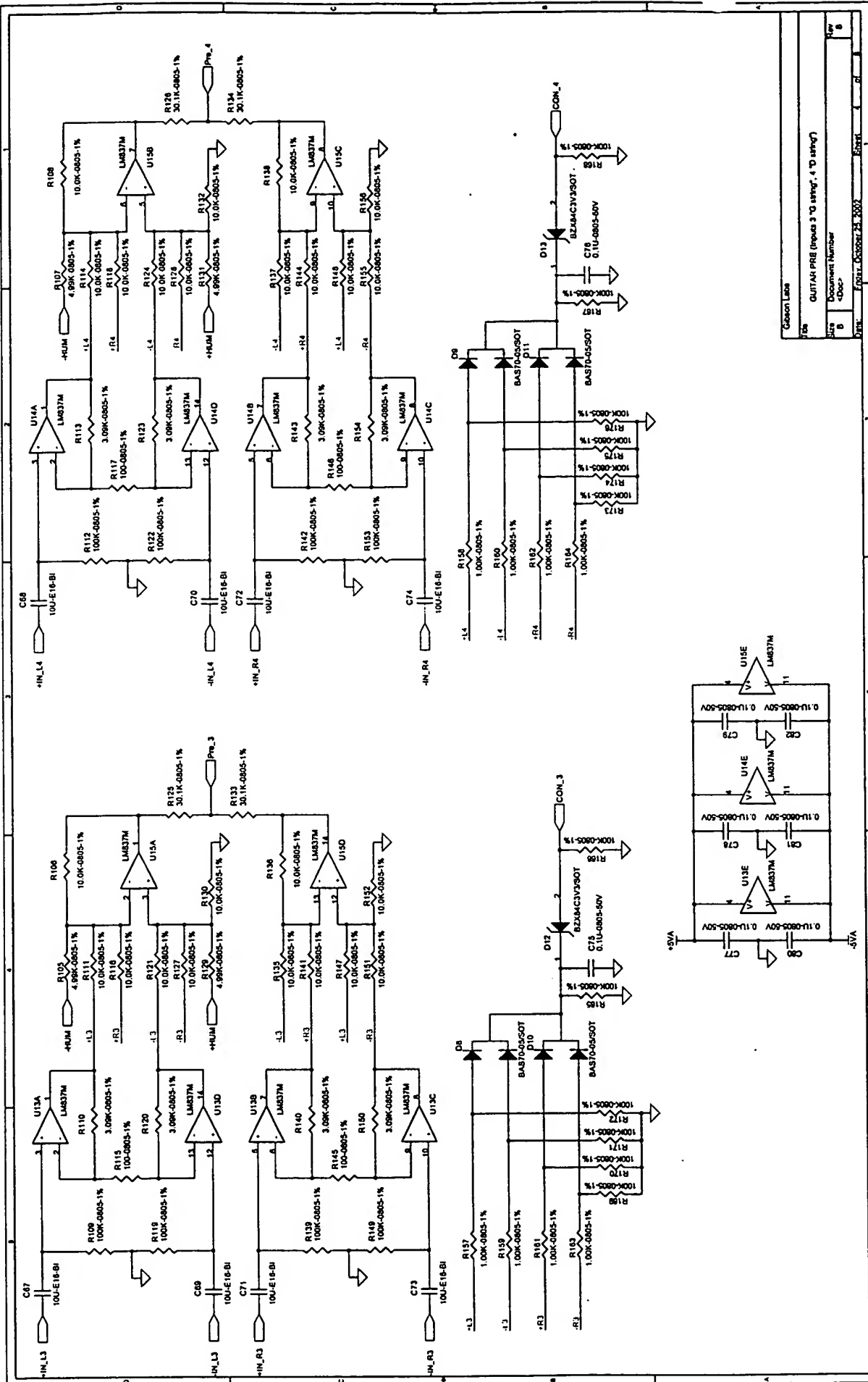


Fig. 30



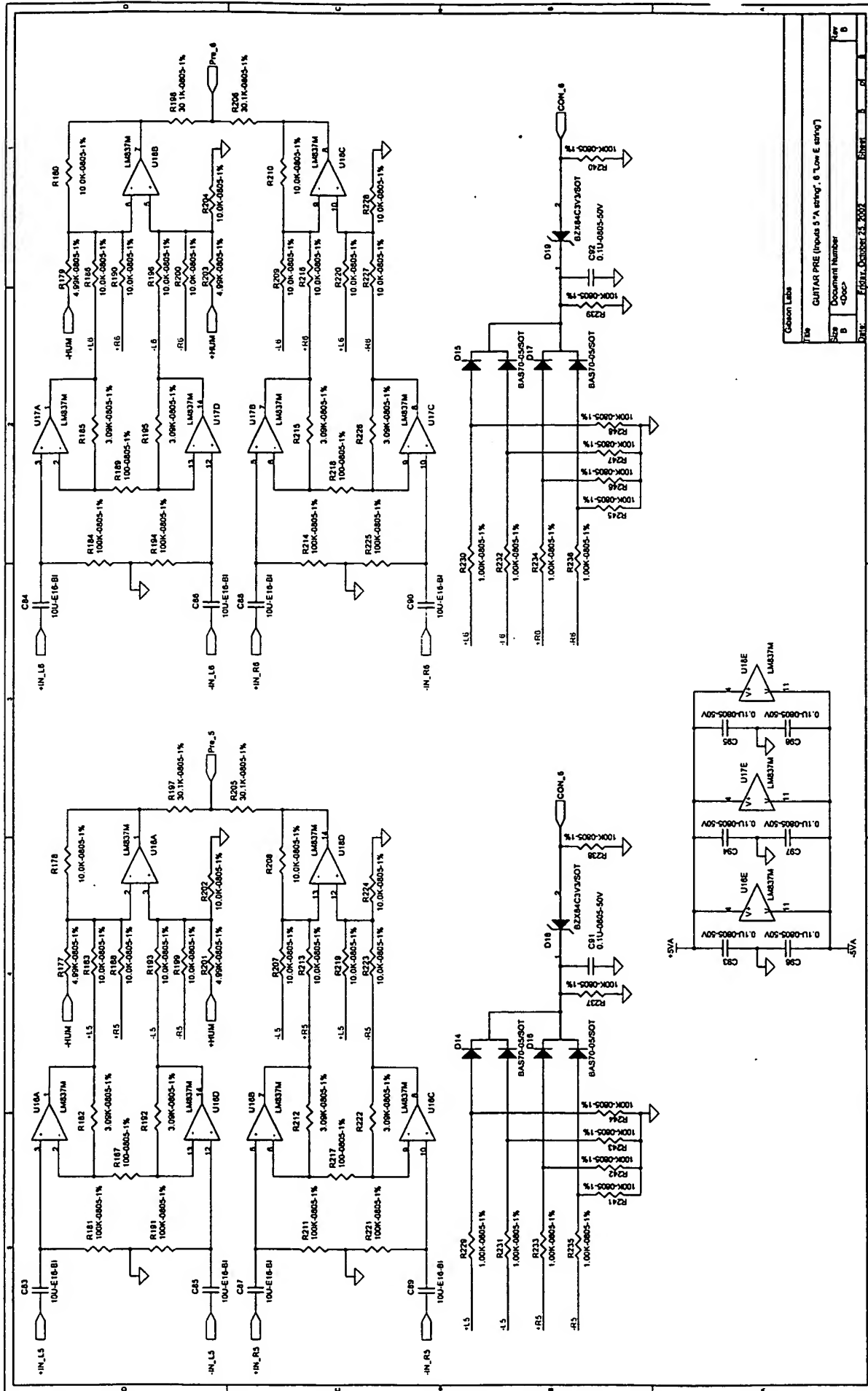
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Date	1957, October 25, 1957

Fig. 31



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By	2002
Sheet	33

Fig. 32



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Fig. 33

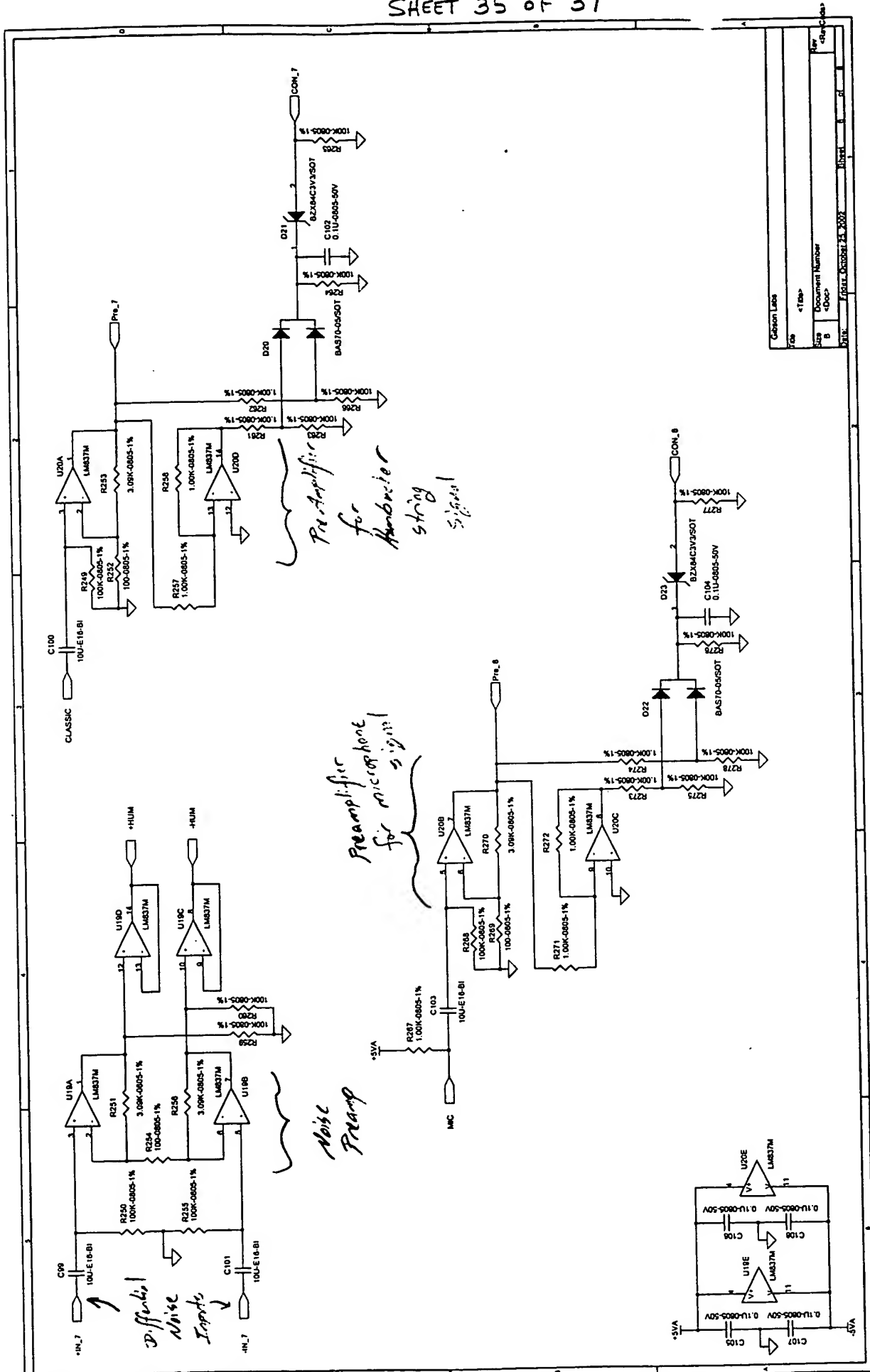


Fig. 34

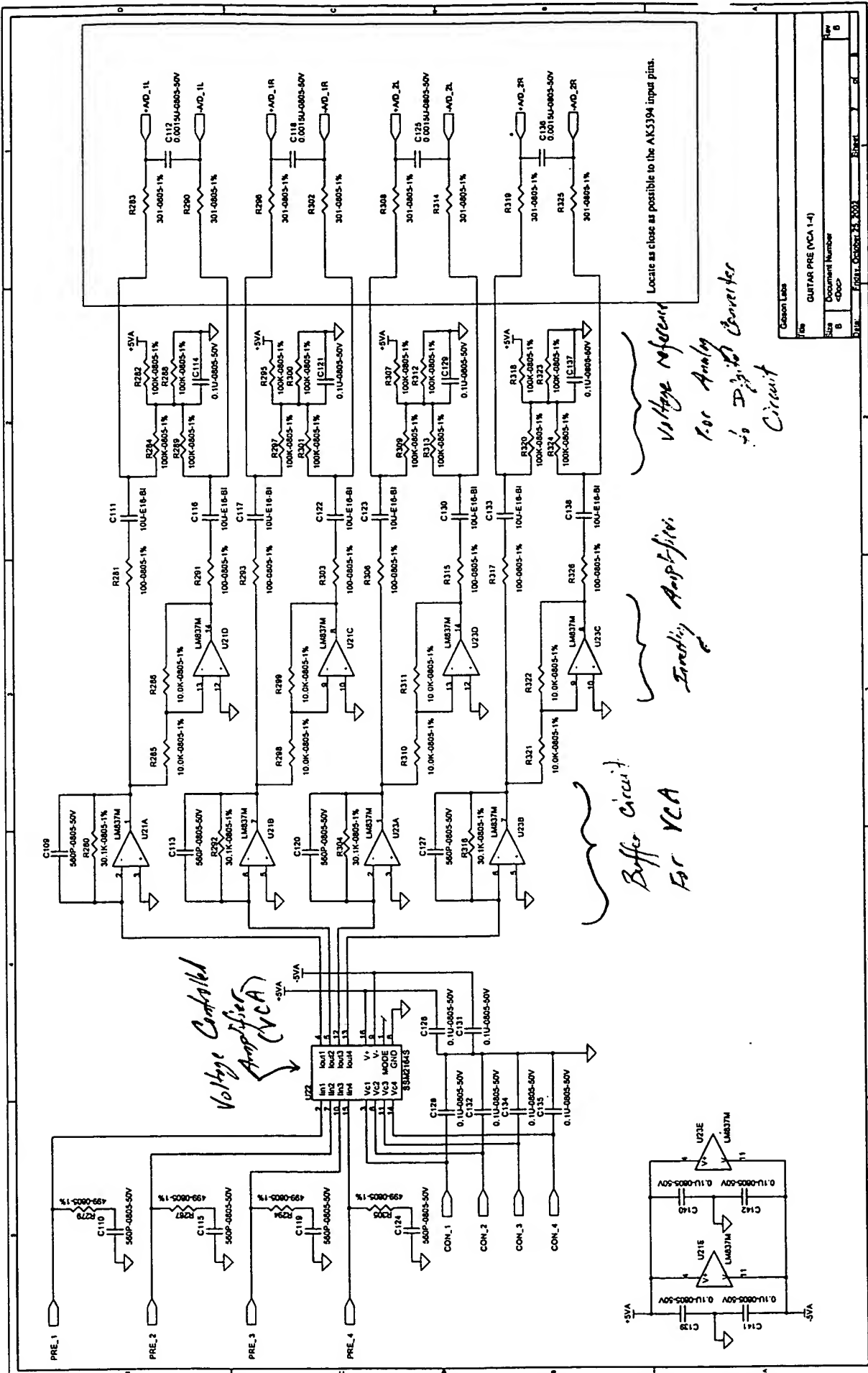
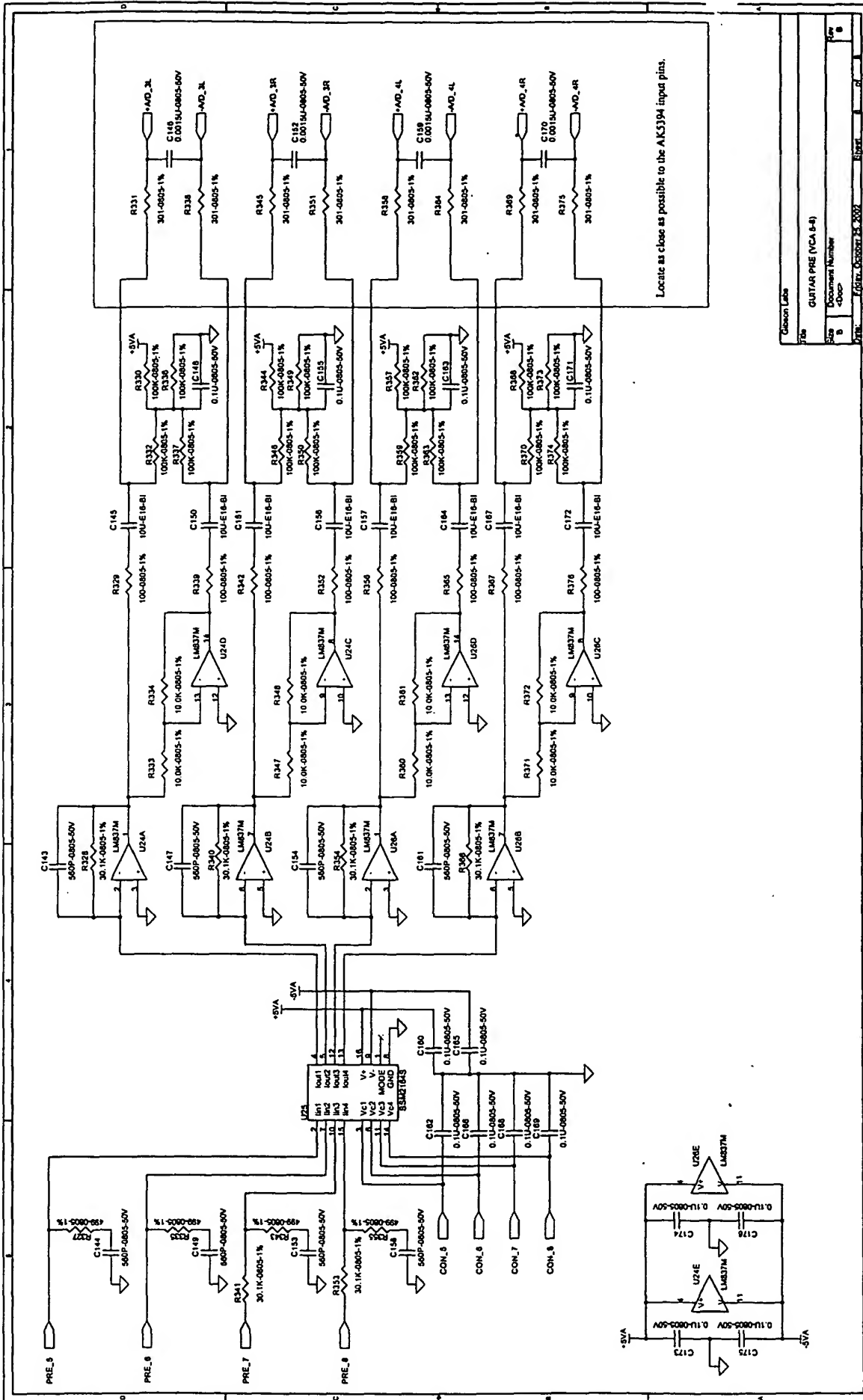


Fig. 35



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Fig. 34